

Form PTO-1449 (Modified)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	APPLICANT Erich Gornick et al	
(37 CFR 1.98(b))	FILING DATE July 23, 2004	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUB- CLASS	FILING DATE IF APPROPRIATE
HL	US	5 4 1 4 5 1 3	05/09/1995				
	US	4 9 5 7 3 6 7	09/18/1990				
	US	4 8 4 1 1 5 0	06/20/1989				
	US	5 2 2 9 3 0 3	07/20/1993				
	US	5 7 7 3 3 1 6	06/30/1998				
	US	6 1 8 1 4 1 6	01/30/2001				
	US	6 2 2 2 1 8 7	04/24/2001				
	US	4 6 8 2 6 0 5	07/28/1987				
HL	US	4 8 1 8 1 1 0	04/40/1989				

FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLA SS	SUB- CLASS	TRANSLATION YES 1 NO
HL	1	0 0 4 7 1 3 6	04/19/2001	German			
	WO	0 0 5 7 1 5 9	09/28/2000	PCT			
	1	9 8 4 0 7 2 5	03/18/1999	German			
	1	9 5 1 6 8 4 2	11/30/1995	German			
	EP	0 6 1 8 4 5 5	05/10/1994	EPO			
	WO	9 7 1 3 3 5 8	04/10/1997	PCT			
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HL		DONALDSON W R ET AL: "Integrated circuit tester using interferometric imaging", Proceedings of the Ugim Symposium, Microelectronics Education for the Future Twelfth Biennial, University/Government/Industry, Microelectronics Symposium (Cat. No. 97CH36030), Proceedings of the Ugim Symposium, Microelectronics Education for the Future, page 107 XP010242546, 1997, New York, NY, USA, IEEE, Usa ISBN: 0-7803-3790-5, figure 1
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EXAMINER	/Hwa Lee/ (10/01/2006)	DATE CONSIDERED
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